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Art Unit: 2111

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address "M" will be executed in the next instruction cycle for eliminating the waiving of
the-abovesaid extra cycle to thereby improve ~~heighten~~ the processing effectiveness. As
shown in Fig. 2, the prior art always fetches two additional instructions because in the
case of a ^{simple} conditional branch instruction, the target address of ^{the} ~~a~~ conditional branch
instruction can be either one of the following two instructions. The pre-fetching of two
instructions continuously while executing the program increases the consumption of
power.

ICSK
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Page 2, amend paragraph [0006] as:

[0006] Nevertheless Although the efficiency is improved in the above method,
more power is consumed during the process of fetching and storing those two
instructions ~~previously, and it is considered still rooms available for improvement of~~
~~power consumption and there is a need to further improve the pre-fetching of~~
instructions for reducing power consumption.

Page 2, amend paragraph [0007] as:

[0007] The primary object of this invention is to provide a kind ~~of architecture of~~
method for fetching microprocessor's instructions. The method which normally pre-
fetches ~~pre-reads~~ a next instruction would pre-fetch ~~pre-read~~ and pre-decode two next
instructions in case it encounters a conditional branch "CALL" instruction so as to waive
unnecessary reading of program memory and reduce power consumption accordingly.

Pages 2-3, amend paragraph [0008] as:

[0008] Another object of this invention is to provide an ~~a kind of~~ architecture of
~~method for practicing the method of~~ fetching microprocessor's instructions. In the process